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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,252	12/26/2001	Toshiyuki Ohtaki	10830-085001	8112

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/033,252	Applicant(s) OHTAKI ET AL.
	Examiner James C Kerveros	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *1-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5 are pending and are presently under examination.

Claim Objections

Claims 1-5 are objected to because of the following informalities:

Claim 1, line 2 and last paragraph line 1, the symbol "/" defining an alternative form should be changed to "or".

Claim 1, line 13, the term "but" should be changed to "and". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "different in time point" recited in claim 1, second, third, fourth and fifth paragraphs, is a relative term which renders the claim indefinite. The term "different in time point" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term fails to properly define the timing relationship for a "pair of judgment strobe pulses" relative to a point in time.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuglin (US 5835506).

Regarding independent Claim 1, Kuglin discloses a circuit tester (10, FIG. 1) for testing an integrated circuit device under test (DUT) 11, comprising:

A first timing generator (34, FIG. 2) sending timing signals to (TEG SH and TEG SL, FIG. 6) associated with a first pin electronics circuit 20, for outputting a pair of judgment strobe pulses (STBH and STBL) at different time, and in synchronism with a test cycle (CYC) pulse which marks the beginning of a test cycle of the IC measuring device, as illustrated by the timing diagram FIG. 7.

A first edge detector (92 and 94) associated with the first pin electronics circuit 20, comprising edge comparator (92) which samples the HIGH and LOW signals in response to the STBH strobe and produces two output signals indicating the sample values and edge comparator 94 which samples the HIGH and LOW signals in response

to the STBL strobe and produces two output bits indicating the sample values in accordance to the judgment strobe pulses, as illustrated by the timing diagram FIG. 7.

A second timing generator identical to the first timing generator associated with a second pin electronics circuit 20 and which provides a pair of judgment strobe pulses as described above and as illustrated by the timing diagram FIG. 7.

A second edge detector identical to the first edge detector (92, 94) associated with the second pin electronics circuit 20 as described above for producing sample values in accordance to the judgment strobe pulses. FIG.1 shows a plurality of identical pin electronics circuits 20, which carry out test activities for the DUT.

A judgment section comprising a first judgment section, such as comparison circuits (102 and 104) for receiving the output signals from the first edge detector (92 and 94) associated with the first pin electronics circuit 20 and a second judgment section such as comparison circuits (102 and 104) for receiving the output signals from the second edge detector (92 and 94) associated with the second pin electronics circuit 20. The comparison circuits (102 and 104) compare the two output bits from the comparison circuit 92 and 94 against expect data bits EXPA and EXPB for determining acceptance/rejection of timing of the data. If there is no match, the comparison circuit sends a FAIL signal to the master sequencer 14 of FIG. 1 and also forwards the two output bits of comparison circuit to an acquisition memory 103.

Kuglin does not explicitly disclose one judgment section for determining acceptance/rejection on the basis of the states of the data detected by the second edge detector and the states of the data strobe detected by the first edge detector.

However, Kuglin discloses a first and a second judgment section, which receives output signals already synchronized by the master clock 22, ROSC, which is used as a timing reference for all devices of tester 10. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the individual judgment sections, as taught by Kuglin, for determining pass or failure condition of multiple IC signal outputs, since employing "Multiple pass" testing reduces the amount of vector data that is needed to test an IC by using all or a part of the vector data which can make efficient use of its vector memory capacity and which can operate at high speeds while employing relatively slow vector memories, (see Kuglin col. 2, lines 35-45).

Regarding Claim 2, Kuglin discloses a pair of judgment strobe pulses (STBH and STBL) outputted from the first timing generator associated with the first pin electronics and another pair of judgment strobe pulses (STBH and STBL) outputted by the second timing generator associated with the second pin electronics, FIG. 7. The time interval between the pair of judgment strobe pulses (STBH and STBL) corresponding to the first and second timing generator is set by the first and second comparison circuits (102 and 104), respectively.

Regarding Claim 3, Kuglin discloses establishing between timing at which the first timing generator outputs each of the judgment strobe pulses (STBH and STBL) and timing at which the second timing generator outputs (STBH and STBL) corresponding one of the judgment strobe pulses, using first and second comparison circuits (102 and 104) for the acquisition memory 103, respectively. FIG. 7.

Regarding Claim 4, Kuglin discloses a plurality of circuit blocks pin electronics circuits (20, FIG. 1) each including the second timing signal generator (34, FIG. 2), the second edge detector (92 and 94) and the judgment section (102 and 104) of FIG. 6.

Regarding Claim 5, Kuglin discloses a relationship is established among judgment strobe pulses (STBH and STBL) outputted from the second timing generators (34, FIG. 2), included pin electronics circuits (20, FIG. 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
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Date: 28 May 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner